CLAIMS

1. A voltage discharge circuit adapted to be coupled to a first node and a second node and adapted to receive first and second discharge signals, the voltage discharge circuit operable in a first mode in response to the first discharge signal to couple the first node to the second node and to discharge voltages on the first and second nodes at a first rate, and operable in a second mode in response to the second discharge signal to discharge the voltages on the first and second nodes at a second rate.

2. The voltage discharge circuit of claim 1 wherein the first node comprises an array source and the second node comprises a p-well drive.

3. The voltage discharge circuit of claim 1 wherein the first rate comprises a controlled discharge of current from the first and second nodes to ground.

4. The voltage discharge circuit of claim 1 wherein the second rate comprises an uncontrolled discharge of current from the first and second nodes to ground.

5. The voltage discharge circuit of claim 1 wherein the first discharge signal goes active to initiate the first mode and couple the first node to the second node, and the first discharge signal remains active during the second mode.

6. The voltage discharge circuit of claim 1 further adapted to be coupled to a third node, and operable in response to the first discharge signal to coupled the third node to ground to discharge a voltage on the third node, and wherein the first and second nodes are capacitively coupled to the third node.

7. The voltage discharge circuit of claim 1 wherein the first mode has a first duration sufficient to allow the voltages on the first and second nodes to discharge to a threshold voltage having a magnitude that is substantially near ground.

8. The voltage discharge circuit of claim 1 wherein the circuit maintains the first node coupled to the second node during the second mode of operation.

9. An erase discharge circuit, comprising:

a first switching circuit coupled between the array source and p-well drive and adapted to receive a first discharge signal, the first switching circuit operable to couple the array source to the p-well responsive to the first discharge signal;

a second switching circuit adapted to receive the first discharge signal and coupled between the array source and p-well drive and ground, the second switching circuit operable in response to the first discharge signal to control the flow of current from the array source and p-well drive to ground; and

a third switching circuit adapted to receive the second discharge signal and coupled between the array source and p-well drive and ground, the third switching circuit operable in response to the second discharge signal to couple the array source and p-well drive to ground.

10. The erase discharge circuit of claim 9 wherein the first switching circuit is operable to present an impedance having a value that is a function of a voltage of the first discharge signal.

11. The erase discharge circuit of claim 9 wherein the first and third switching circuits each comprises a transistor.

12. The erase discharge circuit of claim 9 wherein the second switching circuit comprises a diode-coupled transistor that is coupled between the array source and p-well drive and ground responsive to the second discharge signal being active and is isolated from the array source and p-well drive responsive to the second discharge signal being inactive.

13. The erase discharge circuit of claim 9 further including a fourth switching circuit adapted to be coupled to a word line and ground, and operable in response to the first discharge signal to couple the word line to ground.

14. An erase discharge circuit, comprising:

a control circuit adapted to receive a first discharge signal and a second discharge signal and operable in a first mode responsive to the first discharge signal being active to develop a first activation signal and to control a rate of increase of a magnitude of the first activation signal, and operable in a second mode responsive to the second discharge signal being active to develop a second activation signal and to control a rate of increase of a magnitude of the second activation signal;

a first switching circuit coupled between the array source and p-well drive and coupled to the control circuit to receive the first activation signal, the first switching circuit operable to present an impedance having a value that is a function of the magnitude of the first activation signal;

a current-limiting device having a first node coupled to ground and having a second node, the current limiting device allowing a current to flow from the second node to the first node;

a second switching circuit coupled between the array source and p-well drive and the second node of the current-limiting device, and being coupled to the control circuit to receive the first activation signal, the second switching circuit operable to present an impedance having a value that is a function of the magnitude of the first

activation signal to discharge the array source and p-well drive at a first rate, the first rate having a value that is a function of the current through the current-limiting device and the impedance of the second switching circuit; and

a third switching circuit coupled to the control circuit to receive the second discharge signal and coupled to the first and second nodes of the current-limiting device, the third switching circuit operable in response to the second discharge signal to couple the second node to ground to discharge the array source and p-well drive at a second rate.

15. The erase discharge circuit of claim 14 wherein the first and second switching circuits each comprises a transistor.

16. The erase discharge circuit of claim 14 wherein the current-limiting device comprises a diode-coupled transistor.

17. The erase discharge circuit of claim 14 further including a fourth switching circuit adapted to be coupled to a word line and ground, and operable in response to the first discharge signal to couple the word line to ground.

18. An erase discharge circuit adapted to be coupled to the array source and p-well drive of a block of memory cells and adapted to receive first and second discharge signals, the erase discharge circuit operable in a first mode in response to the first discharge signal to couple the array source to the p-well drive and to discharge current from the array source and p-well drive at a first rate until the voltages on the array source and p-well drive are within a threshold value of a reference voltage, the threshold value being substantially less than an initial value of the voltages on the array source and p-well drive, and the erase discharge circuit operable in a second mode in response to the second discharge signal to discharge current from the array source and p-well drive at a second rate

until voltages on the array source and p-well drive are approximately equal to the reference voltage.

19. The erase discharge circuit of claim 18 wherein the first rate comprises a controlled discharge of current from the array source and p-well drive to ground.

20. The erase discharge circuit of claim 18 wherein initial value of the voltages on the array source and p-well drive comprises a programming voltage VPP, and the threshold value comprises a threshold voltage VT of a diode-coupled transistor.

21. The erase discharge circuit of claim 18 wherein the second rate comprises an uncontrolled discharge of current from the array source and p-well drive to ground.

22. The erase discharge circuit of claim 18 wherein the first discharge signal goes active to initiate the first mode and couple the array source to the p-well drive, and the first discharge signal remains active during the second mode.

23. The erase discharge circuit of claim 18 wherein the second rate comprises a discharge rate of current from the array source and p-well drive to ground, the second rate having a value that is a function of the voltages on the array source and p-well drive.

24. The erase discharge circuit of claim 18 further adapted to be coupled to a word line, and operable in response to the first discharge signal to couple the word line to ground.

25. The voltage discharge circuit of claim 18 wherein the circuit maintains the array source coupled to the p-well drive during the second mode of operation.

26. An erase discharge circuit adapted to be coupled to the array source and p-well drive of a block of memory cells and adapted to receive first and second discharge signals, the erase discharge circuit operable in a first mode in response to the first discharge signal to couple the array source to the p-well drive and to discharge current from the array source and p-well drive for a first time until the voltages on the array source and p-well drive are within a threshold value of a reference voltage, the threshold value being substantially less than an initial value of the voltages on the array source and p-well drive, and the erase discharge circuit operable in a second mode in response to the second discharge signal to discharge current from the array source and p-well drive for a second time until voltages on the array source and p-well drive are substantially equal to the reference voltage.

27. The erase discharge circuit of claim 26 wherein initial value of the voltages on the array source and p-well drive comprises a programming voltage VPP, and the threshold value comprises a threshold voltage VT of a diode-coupled transistor.

28. The erase discharge circuit of claim 26 wherein the reference voltage comprises ground.

29. The erase discharge circuit of claim 26 wherein the first discharge signal goes active to initiate the first mode and couple the array source to the p-well drive, and the first discharge signal remains active during the second mode.

30. The erase discharge circuit of claim 26 further adapted to be coupled to a word line, and operable in response to the first discharge signal to couple the word line to ground during the first and second modes.

31. A flash memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a flash memory-cell array coupled to the address decoder, control circuit, and read/write circuit, and including an array source and p-well drive; and

an erase discharge circuit coupled to the array source and p-well drive and coupled to the control circuit to receive first and second discharge signals, the erase discharge circuit operable in a first mode in response to the first discharge signal to couple the array source to the p-well drive and to discharge voltages on the array source and p-well drive at a first rate, and operable in a second mode in response to the second discharge signal to couple the array source to the p-well drive and to discharge the voltages on the array source and p-well drive at a second rate.

32. The flash memory device of claim 31 wherein the erase discharge circuit is further coupled to word lines of the memory-cell array and is operable responsive to the first discharge signal to couple selected word lines to ground.

33. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a flash memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a flash memory-cell array coupled to the address decoder, control circuit, and read/write circuit, and including an array source and p-well drive; and

an erase discharge circuit coupled to the array source and p-well drive and coupled to the control circuit to receive first and second discharge signals, the erase discharge circuit operable in a first mode in response to the first discharge signal to couple the array source to the p-well drive and to discharge voltages on the array source and p-well drive at a first rate, and operable in a second mode in response to the second discharge signal to couple the array source to the p-well drive and to discharge the voltages on the array source and p-well drive at a second rate.

34. The computer system of claim 33 wherein the erase discharge circuit is further coupled to word lines of the memory-cell array and is operable responsive to the first discharge signal to couple selected word lines to ground.

35. A method of discharging first and second voltages on first and second nodes, respectively, the method comprising:

coupling the first node to the second node;

discharging the voltages on the first and second nodes at a first rate; and

discharging the first and second voltages at a second rate.

36. The method of claim 35 wherein discharging the voltages on the first and second nodes at a first rate comprises discharging current from the first and second nodes at rate defined by the current-voltage characteristics of a diode-coupled MOS transistor.

37. The method of claim 35 wherein discharging the first and second voltages at a second rate comprises coupling the first and second nodes to a reference voltage node.

38. The method of claim 35 wherein the first and second nodes comprise an array source node and a p-well drive node, respectively.

39. A method of discharging first, second, and third voltages on first, second, and third nodes, respectively, the first and second nodes being electrically coupled to the third node, the method comprising:

coupling the first node to the second node;

discharging current from the third node;

discharging current from the first and second nodes;

controlling a rate of the discharge of current from the first and second nodes, the rate being controlled to reduce an influence of the discharge of current from the first and second nodes on the voltage on the third node; and

discharging current from the first and second nodes at a second rate.

40. The method of claim 39 wherein controlling a rate of the discharge of current from the first and second nodes comprises discharging current from the first and second nodes at rate defined by the current-voltage characteristics of a diode-coupled MOS transistor.

41. The method of claim 39 wherein discharging current from the first and second nodes at a second rate comprises coupling the first and second nodes to a reference voltage node, and wherein the discharge of current from the third node comprises coupling the third node to the reference voltage node.

42. The method of claim 39 wherein the first and second nodes comprise an array source node and a p-well drive node, respectively, and the third node comprises a word line node.